Data Sheet

SV6158

Single-chip IEEE 802.11b/g/n WLAN SoC with SDIO Interface

General Description

The SV6158 is a fully integrated SoC with 2.4GHz band 1T1R 11b/g/n Wi-Fi and MCU. A single chip MCU SoC targets for applications requiring optimal RF performance, strong security, low power consumption, and small form-factor with minimal external components. Equipped with a proven popular SDK, the SV6158 provides customers a fast time to market solution by leveraging existing software eco system, and still keep possibilities for product differentiation.

The SV6158 integrated the Balun, T/R switch, LNA, PA with advanced architecture enhancement to achieve great receive sensitivity for noisy home scenarios.

The SV6158's highly integrated on-chip Power Management Unit (PMU) supports 3.3~5V wide range supply voltage switching regulators and LDOs to provide noise isolation in between digital and analog domains minimizing external Bill of Material (BoM).

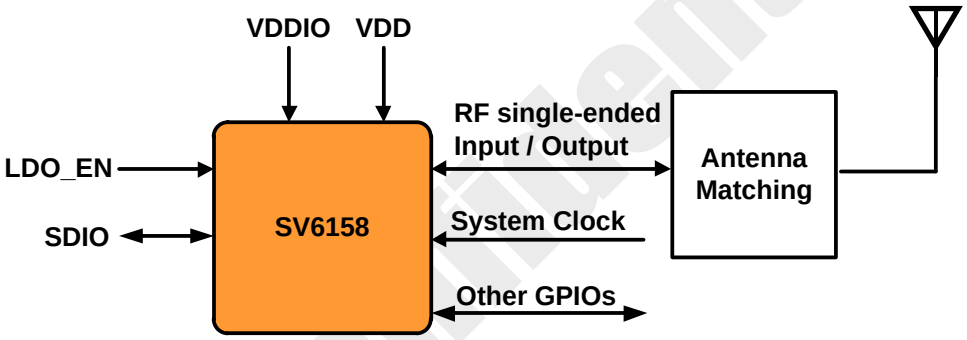
The SV6158 features an application processor subsystem based on Andes D10F 32-bit RISC floating point core which runs at up to 320MHz. The chip includes up to 384KB of embedded SRAM, split among D10F's local TCMs and system SRAM. The entire 384KB SRAM is peripheral addressable.

The SV6158 has a built-in hardware crypto engine, a True Random Number Generator (TRNG) and a 2304b e-fuse block for storing chip-specific information. This combining with high efficiency security middleware library, including Wi-Fi WPA3, the SV6158 builds strong secure system products for smart home applications.

The SV6158 has an average of 390uA DTIM3 current, 33mA receiving current and 212mA transmitting current.

SV6158 Key Points

- IEEE 802.11 b/g/n compliant
- TX power +20 dBm (at pin)
- RX sensitivity -97.5 dBm (at pin)
- Single power supply, range from 3.3 ~ 5V
- Security subsystem
  - AES/SHA/ECC HW crypto engine
  - 2304b e-fuse, TRNG
  - support Wi-Fi Alliance WPA3
- CPU core speed up to 320MHz
- Internal SRAM up to 384KB
- Low power feature
  - DTIM3: 390uA
  - STA/AP: 55mA (Tx 3Mbps, Continue Rx, 2min average)
- Support 24/26/40 MHz crystal oscillator
- Internal 32.768 KHz RC clock with calibration
- Package: QFN32, 4x4 mm, 0.4mm pitch
- Temperature range: -40°C to +85°C



SV6158 System Block Diagram

Liability Disclaimer

Shenzhen iComm Semiconductor Co., Ltd. Reserves the right to make changes without further notice to the product. Shenzhen iComm Semiconductor Co., Ltd. Does not assume any liability arising out of the application or use of any product or circuits described herein.

Revision History

Version	Date	Description
0.1	2020/11/05	Draft
0.2	2020/12/07	• Added 错误!未找到引用源。 • Added BLE Function • Added ch.2.4 Power-on Sequence • Added ch.3 Interface Description • Modified Table 6: ESD Specifications • Modified Table 11:Greenfield changed to Mixed mode • Modified Table 17: Pinmux for SV6158 • Modified 10 Ordering Information • Modified Table 8: Recommended Operating Conditions and DC Characteristics • Modified Table 9, Table 10 for Frequency value and OSCIN Input Voltage Max. • Modified Table 12,Table 13
0.3	2021/03/17	• Modified Figure 2: SV6158 typical Power Connection • Modified Table 8: Recommended Operating Conditions and DC Characteristics • Added SV6158-M
0.4	2021/03/31	• Modified Table 11: Added Rx Sensitivity (HT40)
0.5	2021/06/09	• Added I/O current • Modified Table 12/Table 13: OFF mode current,DTIM1 current,DTIM3 current • Remove part number SV6158-B
0.6	2021/08/12	• Correct Page1/2 DTIM3 current data
1.0	2021/11/03	• Release
1.1	2022/01/20	• Corrected Table 3: Absolute Maximum Ratings • Modified Table 5: The thermal characteristics of the SV6158 • Modified Table 8: Recommended Operating Conditions and DC Characteristics • Remove part number SV6158-M
1.1	2022/03/09	• Remove BLE part

Table of Contents

Lists of Tables

Lists of Figures

1 System Overview

1.1 System Block Diagram

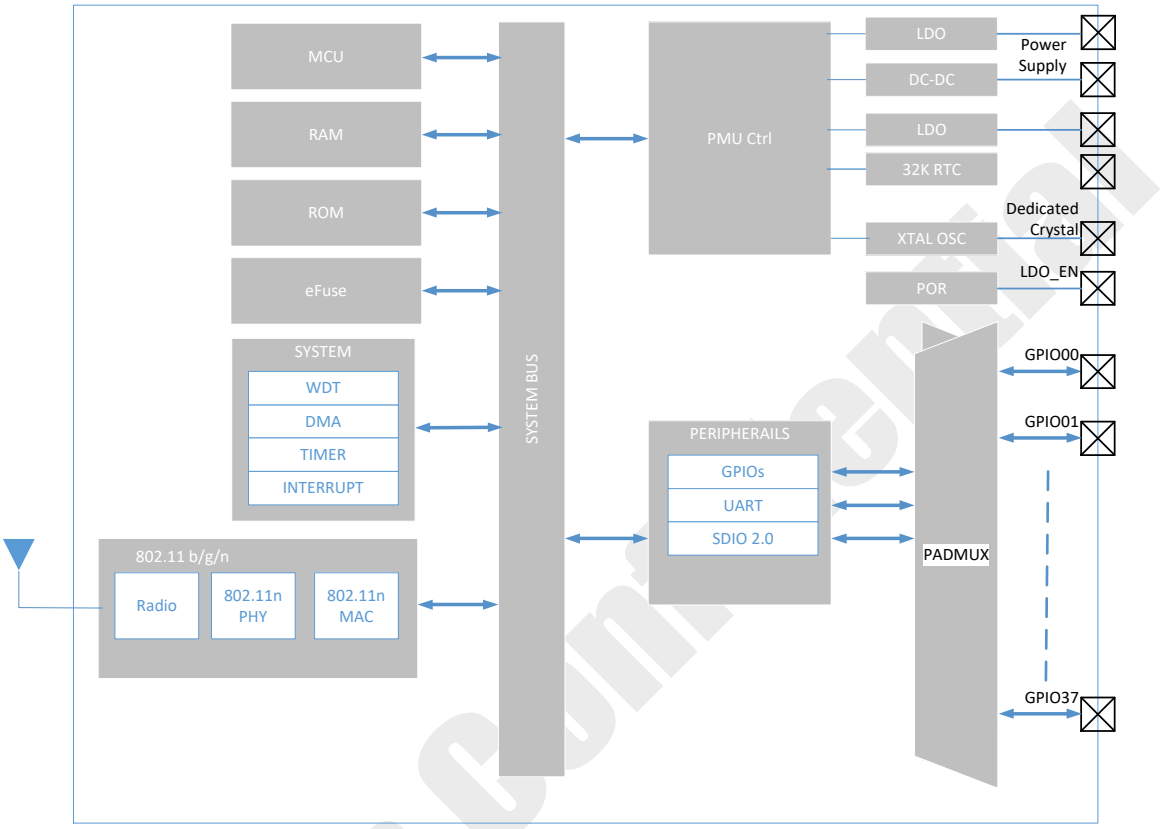


Figure 1: SV6158 Block Diagram

1.2 General Description

The SV6158 WLAN SoC is designed to support IEEE 802.11 b/g/n single spatial stream. It is designed with the state of-the-art techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The SV6158 WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and to achieve extreme low power consumption at sleep state to extend the battery life. The SV6158 WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.

1.3 WLAN FEATURES

- IEEE 802.11 b/g/n 1T1R compliant
- IEEE 802.11 d/e/i/k/r/w supported
- Support 20/40MHz up to MCS7 150Mbps
- 802.11n features supported
  - A-MPDU Tx & Rx for high MAC throughput
  - Support immediate Block-Ack
- STA, SoftAP and Sniffer modes supported
- Concurrent AP + STA supported
- Ad-hoc, peer-to-peer and Wi-Fi Direct modes supported
- Low power Tx/Rx for short range scenario
- Low power beacon listen mode
- Low power dormant mode
- WFA features
  - WEP/WPA/WPA2/WPA3
  - WMM
- Short Guard Interval for 802.11n optimal performance
- Greenfield mode for 802.11n optimal performance
- STBC in RX mode
- Tx power: +20 dBm
- Rx sensitivity: -97.5 dBm
- Integrated Balun, T/R switch, LNA and PA for 2.4GHz
- Enhanced and robust sensitivity for wider coverage range
- Supports calibration algorithm to handle non-ideal effects from CMOS RF block

1.4 SYSTEM

- Andes Technology D10F processor w/ ILM/DLM and I-cache/D-cache
- DSP instruction set with SIMD
- Tightly coupled single precision floating point unit (FPU)
- Dedicated 16KB I-cache/D-cache supported
- Memory Protection Unit (MPU) supported
- 128KB ROM and up to 384KB SRAM for Instruction and data SRAM in total
- Low power Dormant mode with 16KB retention SRAM
- Low power Shut-Down mode
- Integrated on-chip Power Management Unit (PMU) support 3.3~5V wide range
- Security and encryption
- AES/SHA/ECC hardware acceleration
- Integrated True Random Number Generator
- Integrated 2304b e-fuse and Secure boot
- Suspend/Wake-up manger controller
- 2DMA, each with 8 channels
- Four millisecond timers
- Four microsecond timers
- Two watchdog timers

1.5 HOST INTERFACE

- SDIO 2.0
  - 1bit/4bits mode supported
  - Support Clock up to 50MHz

1.6 SYSTEM CLOCKING AND RESET

The SV6158 has a system clocking block and reset which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to internal modules. The system clocking and reset block also manages resets going to other modules within the device.

1.7 DESIGN FOR TEST

It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

2 POWER SUPPLIES AND POWER MANAGEMENT

2.1 GENERAL DESCRIPTION AND PMU POWER CONNECTION

The power management unit (PMU) contains Low Dropout Regulators (LDOs), buck DC-DC converter and reference bandgap circuit.

The PMU integrates multi-LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line / load regulation, ripple rejection and output noise.

The input voltage of the buck converter is 3.3V. Its output voltage is 1.1V and feeds into the input power of the RF circuit and DLDO which has 0.8V output voltage for all digital circuits.
Figure 2 shows the typical power connection for SV6158. DLDO and some RF circuits are powered by the buck converter output. The VDDIO is a power input which may be 1.8V or 3.3V from the host side. The connection structure is shown in the Figure 2

SV6158 supports 5V input, and internal LDO generates 3.3V through RVD33_OUT for all 3.3V power pins. Figure 3 shows 5V power connection for SV6158. This feature can save one additional LDO component on PCB. The connection structure is shown in the Figure 3

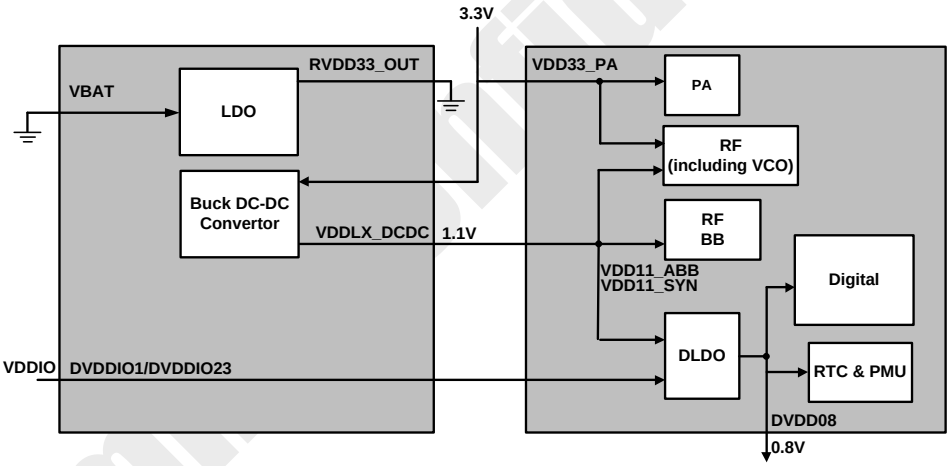


Figure 2: SV6158 typical Power Connection

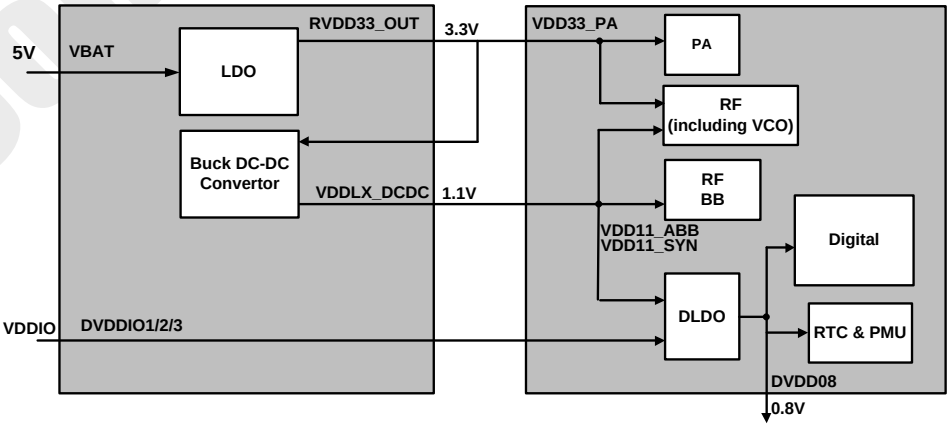


Figure 3: SV6158 Power Connection with Internal LDO

2.2 DLDO

The DLDO is integrated in the PMU to supply digital core. It converts voltage from 1.1V input to 0.8V output which suits the digital circuits. The input is typically connected to the buck's output.

2.3 BUCK CONVERTER

The regulator is a DC-DC step-down converter (buck converter) to source 300 mA (max.) with 1.3V to 1.05V programmable output voltage based on the register setting. It supplies power for the RF circuit and DLDO.

2.4 POWER-ON SEQUENCE

2.4.1 POWER-ON SEQUENCE WITH TYPICAL POWER

Figure 4 shows the VDD33=3.3V power-on sequence of the SV6158 from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept above the threshold voltage. After initial power-on, the LDO_EN signal can be held low to turn off the SV6158 or pulsed low to induce a subsequent reset.

After LDO_EN is asserted, the host starts the power-on sequence of the SV6158. From that point, the typical SV6158 power-on sequence is shown below:

1. Within T1+2.5ms, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

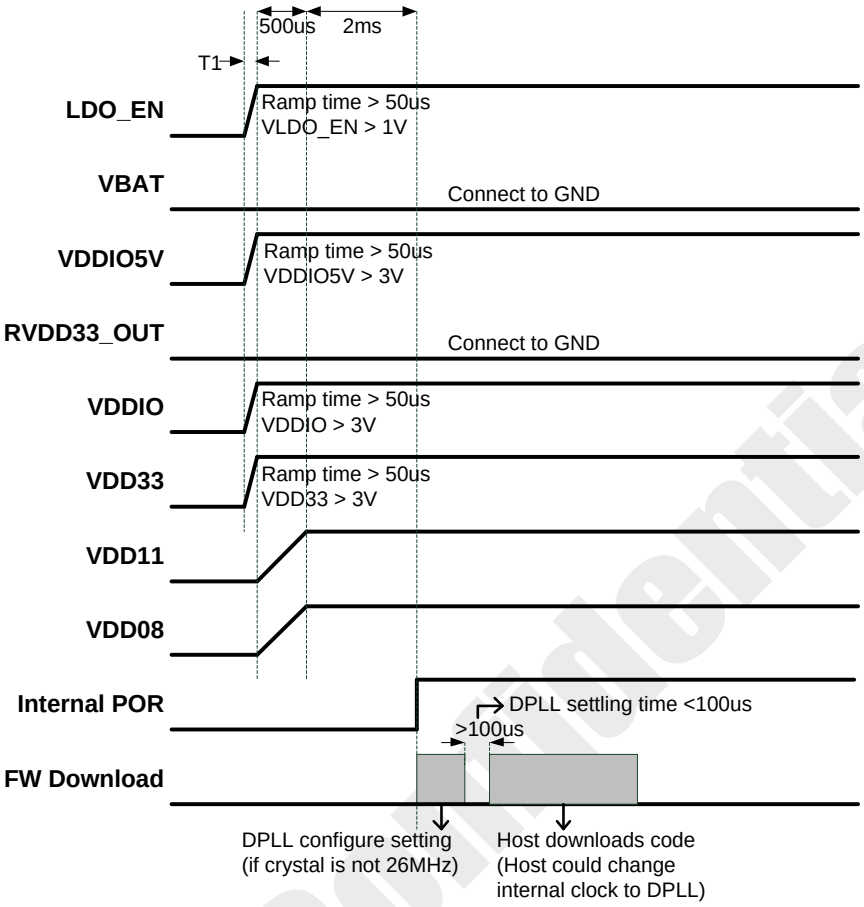


Figure 4: Power-on sequence with typical power

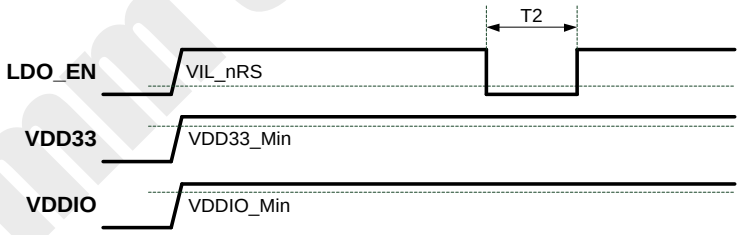


Figure 5: Reset Timing with typical power

2.4.2 POWER-ON SEQUENCE WITH TYPICAL POWER

Figure 6 shows the VBAT=5V power-on sequence of the SV6158 from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level pull high automatically by chip internal VBAT when VBAT input. After initial power-on, the LDO_EN signal can be held low to turn off the SV6158 or pulsed low to induce a subsequent reset.

After LDO_EN is asserted, the host starts the power-on sequence of the SV6158. From that point, the typical SV6158 power-on sequence is shown below:

1. Within T1+3.5ms, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

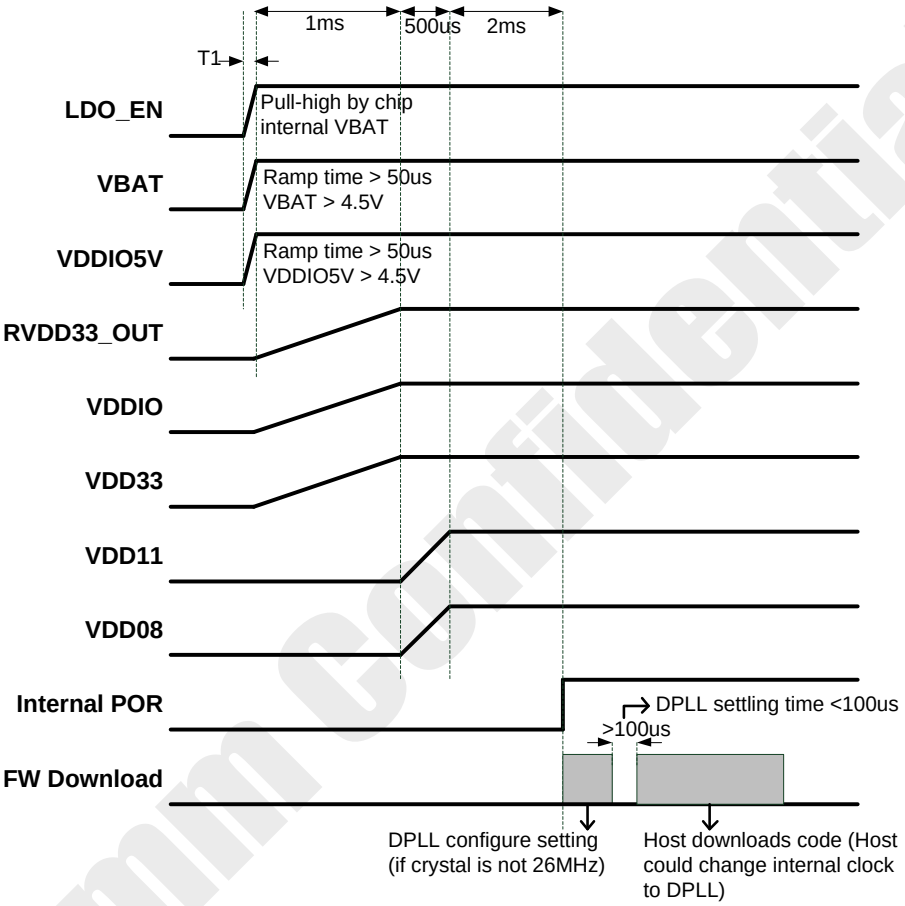


Figure 6: Power-on sequence with Internal LDO

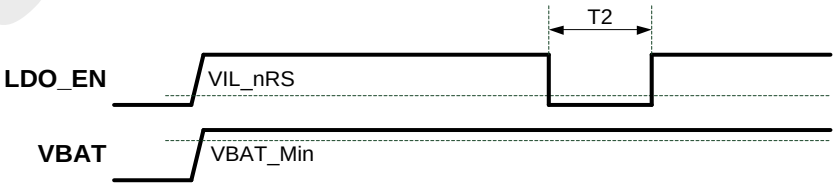


Figure 7: Reset Timing with Internal LDO

Table 1: Reset Timing Parameters

Parameters	Description	Min.	Unit
T_2	Duration of LDO_EN signal level < VIL_Nrst(refer to its value in Table 8: Recommended Operating Conditions and DC Characteristics) to reset the chip	500	us

2.5 RESET CONTROL

The SV6158 **LDO_EN** pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SV6158 is in off mode waiting for host communication. Until then, the MAC, Baseband modem, and MCU subsystem blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SV6158 turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

3 INTERFACE DESCRIPTION

3.1 SDIO CHARACTERISTICS

SDIO is compliant to SDIO specification version 2.0, supporting 1-bit and 4-bit data transfer mode, and compliant to high speed SD Bus

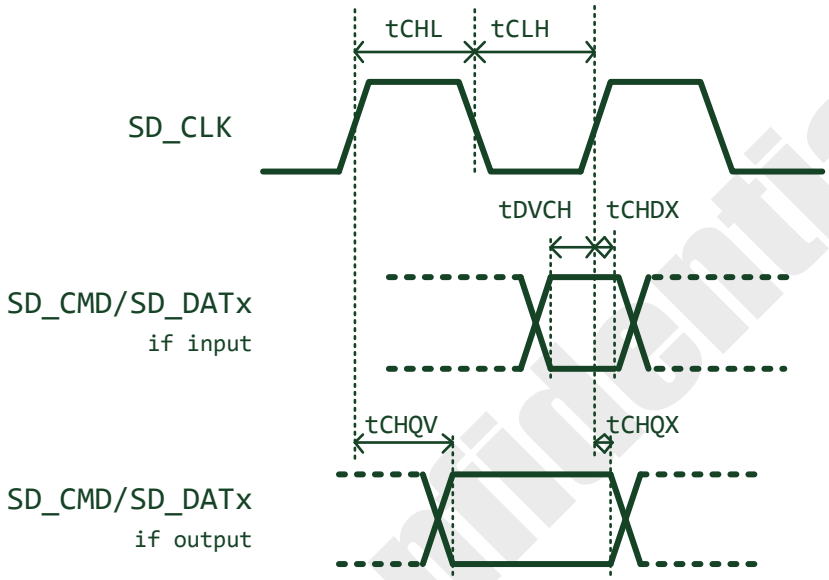


Figure 8: SDIO Timing

Table 2: SDIO Timing Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
SDIO clock frequency	–	(TBD)		50	MHz
SDIO clock high time	Tchl	7	–	-	ns
SDIO clock low time	Tclh	7	-	-	ns
SDIO input setup time	Tdvch	6	-	-	ns
SDIO input hold time	Tchdx	2	-	-	ns
SDIO output delay	Min.: Tchqx, Max.: Tchqv	2.5	-	14	ns

4 DC CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings in Table 3 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 3: Absolute Maximum Ratings

Symbol (domain)	Description	Max Rating	Unit
AVDD11_SX	VDD input for analog 1.1V	-0.3 to 1.8	V
AVDD11_RF	VDD input for analog 1.1V	-0.3 to 1.8	V
AVDD33_SX	VDD input for external components I/O control	-0.3 to 3.6	V
AVDD33_PA	VDD input for external components I/O control	-0.3 to 3.6	V
AVDD33_TX	VDD input for external components I/O control	-0.3 to 3.6	V
DVDDIO1	VDD input for GPIO pins	-0.3 to 3.6	V
DVDDIO2	VDD input for GPIO pins	-0.3 to 3.6	V
DVDDIO3	VDD input for GPIO pins	-0.3 to 3.6	V
DVDD08_DIG	VDD output for internal digital circuit	-0.3 to 1.0	V
DVDD11_DIG	VDD input for digital circuit's LDO	-0.3 to 1.4	V
VBAT	VDD input for VBAT	-0.3 to 5.5	V
AVDD33_DCDC	VDD input for DCDC	-0.3 to 3.6	V

4.2 ENVIRONMENTAL RATINGS

The environmental ratings are shown in Table 4

Table 4: Environmental Ratings

	Part Number	Value	Units
Operating Temperature(T_A)	SV6158	-40 to +85	°C

4.3 STORAGE CONDITION

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

a) Mounted within 168-hours of factory conditions < 30 **°C** /60%RH
b) Storage humidity needs to maintained at <10% RH
c) Baking is necessary if customer exposes the component to air over 168 hours, baking condition: 125°C / 8hours

4.4 THERMAL CHARACTERISTICS

Table 5: The thermal characteristics of the SV6158

Thermal characteristics without external heat sink in still air condition

Symbol	Description	Typ.	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
θ_{JA}	Thermal Resistance θ_{JA} (°C /W) for JEDEC 4L system PCB	59.9	°C/W
θ_{JC}	Thermal Resistance θ_{JC} (°C /W) for JEDEC 4L system PCB	40.1	°C/W
Ψ_{Jt}	Thermal Characterization parameter Ψ_{Jt} (°C /W) for JEDEC 4L system PCB	0.8	°C/W
	Maximum Lead Temperature (Soldering 10s)	260	°C

Notes: * JEDEC 51-7 system FR4 PCB size: 3" x 4.5" (76.2 x 114.3 mm)

* Thermal characteristics without external heat sink in still air condition

4.5 ELECTROSTATIC DISCHARGE SPECIFICATIONS

This is an ESD sensitive product. Observe precaution and handle with care. Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices.

Table 6: ESD Specifications

ESD Mode	Standard	Pin Name	Value	Unit
Human Body Mode (HBM)	JEDEC EIA/JESD22-A114	All pins exclude XO/XI	±3000	V
		XO/XI	±2000	V

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process

4.6 POWER-ON HOURS(POH)

This information is provided solely for your convenience and does not extend or modify the warranty provided under iComm's standard terms and conditions for iComm semiconductor products.

Table 7: Power-On Hours

OPERATION CONDITION	Part Number	Power-On Hours(POH)(hours)
T_A up to 85°C [a]	SV6158	87600

a. The TX duty cycle (power amplifier ON time) is assumed to be 10% of the device POH. Of the remaining 90% of the time, the device can be in any other state.

4.7 Recommended Operating Conditions and DC Characteristics

Table 8: Recommended Operating Conditions and DC Characteristics

Domain (Symbol)	Description	Min.	Typ.	Max.	Unit
AVDD11_SX	VDD input for analog 1.1V	0.9	1.1	1.3	V
AVDD11_RF	VDD input for analog 1.1V	0.9	1.1	1.3	V
AVDD33_SX	VDD input for external components I/O control	2.1	3.3	3.46	V
AVDD33_PA	VDD input for external components I/O control	2.1	3.3	3.46	V
AVDD33_TX	VDD input for external components I/O control	2.1	3.3	3.46	V
DVDDIO1	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDDIO2	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDDIO3	VDD input for GPIO pins	1.75	3.3	3.46	V
DVDD08_DIG	VDD output for internal digital circuit		0.8		V
DVDD11_DIG	VDD input for digital circuit's LDO		1.1		V
VBAT with 5v*[a]	VDD input	3.3	5	5.25	V
RVDD33*[a]	VDD output		3.3		V
VBAT with 0v*[b]	VDD input/VDD output		0		V
AVDD33_DCDC	VDD input for DCDC	2.1	3.3	3.46	V
(V_{IL})	Input Low voltage when VDDIO=3.3V	-0.3		0.8	V
(V_{IH})	Input High voltage when VDDIO=3.3V	2		3.6	V
(V_{T+})	Schmitt trigger low to high threshold voltage when VDDIO=3.3V	1.52	1.63	1.77	V
(V_{T-})	Schmitt trigger high to low threshold voltage when VDDIO=3.3V	1.29	1.41	1.56	V
(V_{OL})	Output low voltage when VDDIO=3.3V			0.4	V
(V_{OH})	Output high voltage when VDDIO=3.3V	2.4			V
(R_{PD})	Input weakly pull-down resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull-down option except that GPIO_5 has internal weakly pull-up option				KΩ
(R_{PU})	Input weakly pull-high resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull-down option except that GPIO_5 has internal weakly pull-up option				KΩ
VIH_Nrst	Chip reset release voltage		>1		V
VIL_Nrst	Chip reset voltage		<0.1		V

(I_{OL})	Low level output current @ V_{OL}(max), 8 mA setting	5.2	7.52	10.09	mA
	Low level output current @ V_{OL}(max), 12 mA setting	10.4	15.03	20.2	mA
(I_{OH})	High level output current @ V_{OH}(min), 8 mA setting	6.8	12.08	18.44	mA
	High level output current @ V_{OH}(min), 12 mA setting	12.7	22.64	35.09	mA

*a: In 5v application, VBAT connects to 5V, RVDD33 can provide 3.3V.

*b: In 3.3v application, VBAT connects to 0v, RVDD33 is connected to 0v as well.

5 FREQUENCY REFERENCES

5.1 CRYSTAL OSCILLATOR SPECIFICATIONS

Table 9: Crystal Oscillator Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency	–		24/26/40 MHz		
Crystal load Capacitance	–	–	10		Pf
ESR	–	–	–	70	Ω
Frequency tolerance Initial and over temperature	–	-20	–	20	ppm

5.2 EXTERNAL CLOCK-REQUIREMENTS AND PERFORMANCE

Table 10: External Clock-Requirements and Performance

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency	–		24/26/40 MHz		
OSCIN Input Voltage	AC-couple analog signal	400	–	900	mV_{PP}
Frequency tolerance Initial and over temperature	–	-20	–	20	ppm
Duty Cycle	26MHz clock	40	50	60	%
Phase Noise (802.11b/g)	26MHz clock at 1KHz offset	–	–	–119	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–129	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–134	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–139	dBc/Hz
Phase Noise (802.11n 2.4GHz)	26MHz clock at 1KHz offset	–	–	–125	dBc/Hz
	26MHz clock at 10KHz offset	–	–	–135	dBc/Hz
	26MHz clock at 100KHz offset	–	–	–140	dBc/Hz
	26MHz clock at 1MHz offset	–	–	–145	dBc/Hz

6 ELECTRICAL SPECIFICATIONS

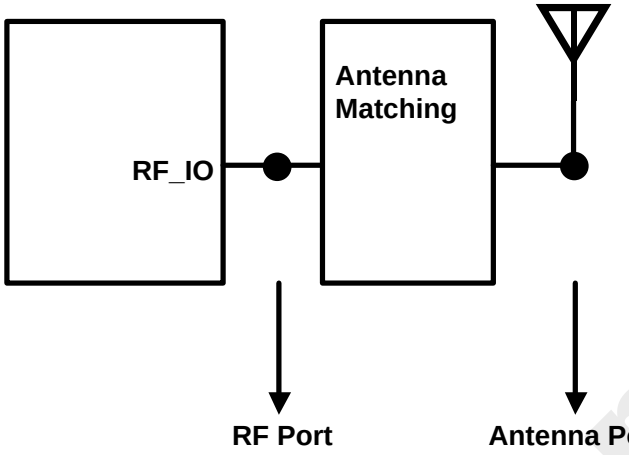


Figure 9: RF Front-End Reference Topology for RF Performance

Note: All specifications are measured at the RF Port unless otherwise specified.

6.1 WLAN RF PERFORMANCE SPECIFICATIONS

Table 11: 2.4G WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1 Mbps		-97.5		dBm
	CCK, 2 Mbps		-94.5		dBm
	CCK, 5.5 Mbps		-92.5		dBm
	CCK, 11 Mbps		-89.0		dBm
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-92.5		dBm
	OFDM, 9 Mbps		-91.5		dBm
	OFDM, 12 Mbps		-89.5		dBm
	OFDM, 18 Mbps		-87.5		dBm
	OFDM, 24 Mbps		-84.5		dBm
	OFDM, 36 Mbps		-81.5		dBm
	OFDM, 48 Mbps		-76.5		dBm
	OFDM, 54 Mbps		-75.5		dBm
Rx Sensitivity (HT20) Mixed mode 800Ns GI Non-STBC	HT20, MCS0		-92.0		dBm
	HT20, MCS1		-89.0		dBm
	HT20, MCS2		-87.0		dBm
	HT20, MCS3		-84.0		dBm
	HT20, MCS4		-81.0		dBm
	HT20, MCS5		-76.0		dBm
	HT20, MCS6		-75.0		dBm
	HT20, MCS7		-73.5		dBm
Rx Sensitivity (HT40) Mixed mode 800nS GI Non-STBC	HT40, MCS0		-88.5		dBm
	HT40, MCS1		-85.5		dBm
	HT40, MCS2		-83.5		dBm
	HT40, MCS3		-80.5		dBm
	HT40, MCS4		-77.5		dBm
	HT40, MCS5		-73		dBm
	HT40, MCS6		-71.5		dBm
	HT40, MCS7		-70.5		dBm
Parameter	**Condition/Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
RX Adjacent Channel Rejection (CCK)	1 Mbps		41		dB
	11 Mbps		41		dB
RX Adjacent Channel Rejection (OFDM)	6 Mbps		39		dB
	54 Mbps		23		dB
RX Adjacent Channel Rejection (HT20)	MCS0		38		dB
	MCS7		21		dB
RX Adjacent Channel Rejection (HT40)	MCS0		30		dB
	MCS7		11		dB

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
TX Output Power (with PADPD)	CCK, 1-11 Mbps		19		dBm
	OFDM, 54 Mbps		15		dBm
	HT20, MCS7		15		dBm
	HT40,MCS7		15		dBm

7 SYSTEM POWER CONSUMPTION

Table 12: Power Consumption at DCDC mode (DCDC buck convertor is enable)

WLAN Operational Modes	Typ.[c]	Unit
OFF[a]	1.5	uA
Rx, CCK, 1 Mbps[e]	33	mA
Rx, OFDM, 54 Mbps[e]	33	mA
Rx, HT20, MCS7[e]	33	mA
Rx, HT40, MCS7[e]	33	mA
Tx, CCK, 1 Mbps@19dBm[d]	212	mA
Tx, OFDM, 54 Mbps@15dBm[d]	182	mA
Tx, HT20, MCS7@15dBm[d]	183	mA
Tx, HT40, MCS7@15dBm[d]	183	mA
Power-saving(MCU_off)[b] , DTIM1	0.85	mA
Power-saving(MCU_off)[b] , DTIM3	0.39	mA

Table 13: Power Consumption at LDO mode (DCDC buck convertor is disable)

WLAN Operational Modes	Typ.[c]	Unit
OFF[a]	1.5	uA
Rx, CCK, 1 Mbps[e]	80	mA
Rx, OFDM, 54 Mbps[e]	80	mA
Rx, HT20, MCS7[e]	80	mA
Rx, HT40, MCS7[e]	80	mA
Tx, CCK, 1 Mbps@19dBm[d]	243	mA
Tx, OFDM, 54 Mbps@15dBm[d]	214	mA
Tx, HT20, MCS7@15dBm[d]	215	mA
Tx, HT40, MCS7@15dBm[d]	215	mA
Power-saving(MCU_off)[b] , DTIM1	1.80	mA
Power-saving(MCU_off)[b] , DTIM3	0.79	mA

a. OFF mode test condition: VBAT=GND, RVDD33=GND, VDD=3.3V, LDO_EN=0V
b. Intra-beacon Sleep when MCU is turn off
c. Conditions: VBAT=GND, RVDD33=GND, VDD=3.3V
d. When the CPU CLK is 160MHz, the Tx current increases 10 mA, when the CPU CLK is 320MHz, the Tx current increases 20 mA
e. When the CPU CLK is 160MHz, the Rx current increases 6 mA, when the CPU CLK is 320MHz, the Rx current increases 12 mA

8 PIN DESCRIPTIONS

8.1 PIN LAYOUT

This section contains a listing of the signal descriptions (see Figure 10 for the SV6158 package pin-out)

Figure 10: SV6158 Pin Assignment –QFN32 (top view)

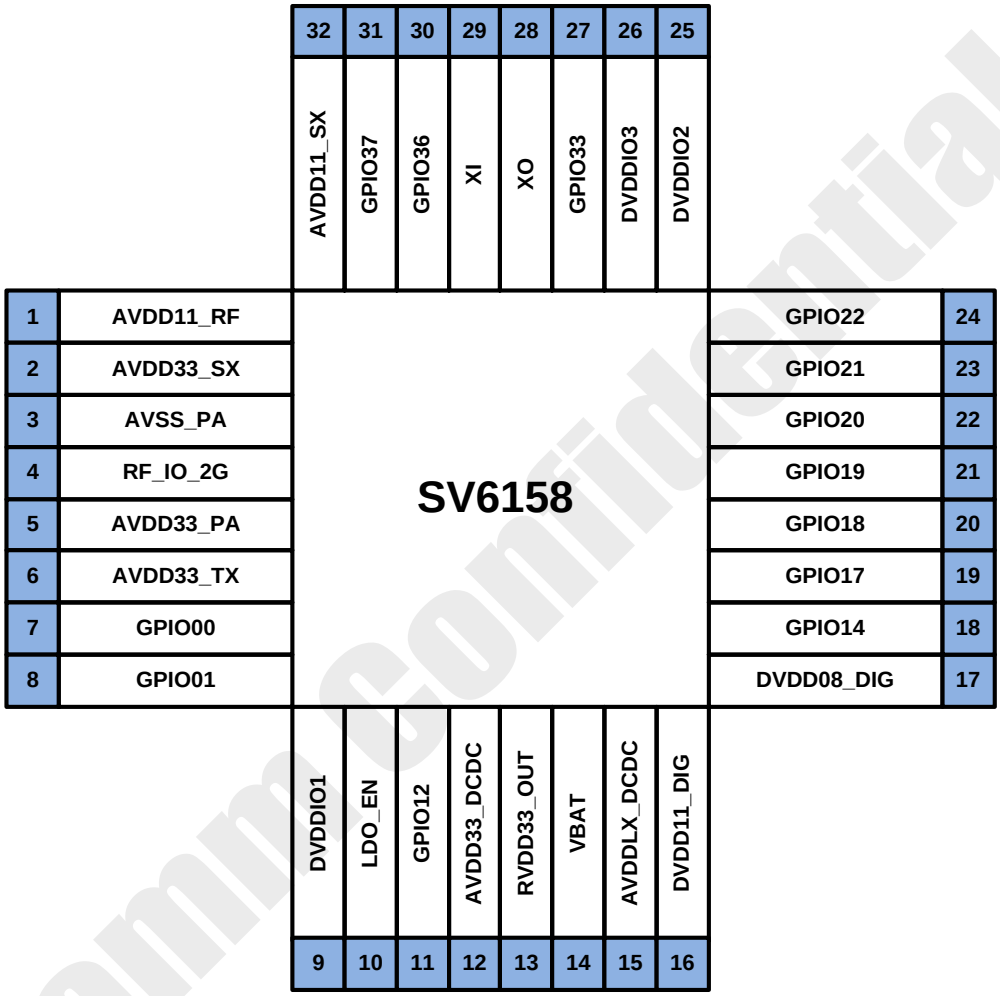


Table 14: SV6158 Pin coordination

Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	AVDD11_RF	2	AVDD33_SX	3	AVSS_PA	4	RF_IO_2G
5	AVDD33_PA	6	AVDD33_TX	7	GPIO00	8	GPIO01
9	DVDDIO1	10	LDO_EN	11	GPIO12	12	AVDD33_DCDC
13	RVDD33_OUT	14	VBAT	15	AVDDLX_DCDC	16	DVDD11_DIG
17	DVDD08_DIG	18	GPIO14	19	GPIO17	20	GPIO18
21	GPIO19	22	GPIO20	23	GPIO21	24	GPIO22
25	DVDDIO2	26	DVDDIO3	27	GPIO33	28	XO
29	XI	30	GPIO36	31	GPIO37	32	AVDD11_SX

8.2 PIN DESCRIPTION

Table 15: SV6158 Package Pin-out

Pin Name	Pin No.	Type*	Description
General purpose I/O			
GPIO00	7	I/O	General Purpose I/O Pins
GPIO01	8	I/O	General Purpose I/O Pins
GPIO12	11	I/O	Strapping Purpose I/O Pins
GPIO14	18	I/O	General Purpose I/O Pins
GPIO17	19	I/O	General Purpose I/O Pins
GPIO18	20	I/O	General Purpose I/O Pins
GPIO19	21	I/O	General Purpose I/O Pins
GPIO20	22	I/O	General Purpose I/O Pins
GPIO21	23	I/O	General Purpose I/O Pins
GPIO22	24	I/O	General Purpose I/O Pins
GPIO33	27	I/O	General Purpose I/O Pins
GPIO36	30	I/O	General Purpose I/O Pins
GPIO37	31	I/O	General Purpose I/O Pins
IO Power			
DVDDIO1	9	P	VIO input
DVDDIO2	25	P	VIO input
DVDDIO3	26	P	VIO input
Reset and Clocks			
LDO_EN	10	I	Reset signal to power down IC
XO	28	O	Output of crystal clock reference
XI	29	I	Input of crystal clock reference
PMU/BUCK			
AVDD33_DCDC	12	P	analog 3.3V input for DCDC
RVDD33_OUT	13	P	Internal LDO output
VBAT	14	P	Power Supply
AVDDLX_DCDC	15	P	DCDC buck regulator: output to inductor
DVDD11_DIG	16	P	DCDC 1.1V output
DVDD08_DIG	17	P	Digital 0.8V input
Wi-Fi radio			
AVDD11_SX	32	P	analog 1.1V input
AVDD11_RF	1	P	analog 1.1V input
AVDD33_SX	2	P	analog 3.3V input
AVSS_PA	3	G	Ground
RF_IO_2G	4	I/O	2.4 GHz RF input & output port
AVDD33_PA	5	P	analog 3.3V input
AVDD33_TX	6	P	analog 3.3V input

* I=Input; O=Output; G=Ground; P=Power

8.3 Mode Selection

Table 16: Mode Selection table

strapping truth table		
GPIO	**Interface mode**	**Description**
GPIO[12]		
0	SDIO	SDIO mode (default)*
1	Reserved	

*No external pull-down resistor is required because internal pull-down is active during power up.

8.4 Function Selection For SV6158

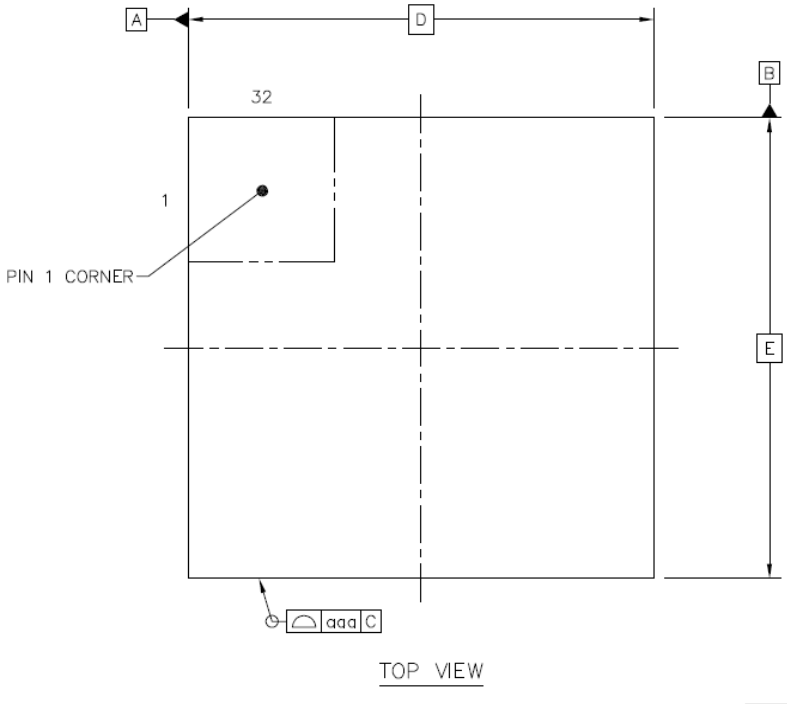
After bootstrap, the SV6158 provides a pad multiplex switching from the bootstrap function to selected I/O function by register signals. There is a condition to leave bootstrap function. That is switching to GPIO first then switching to select I/O function. The table shows the all I/O functions for each PAD.

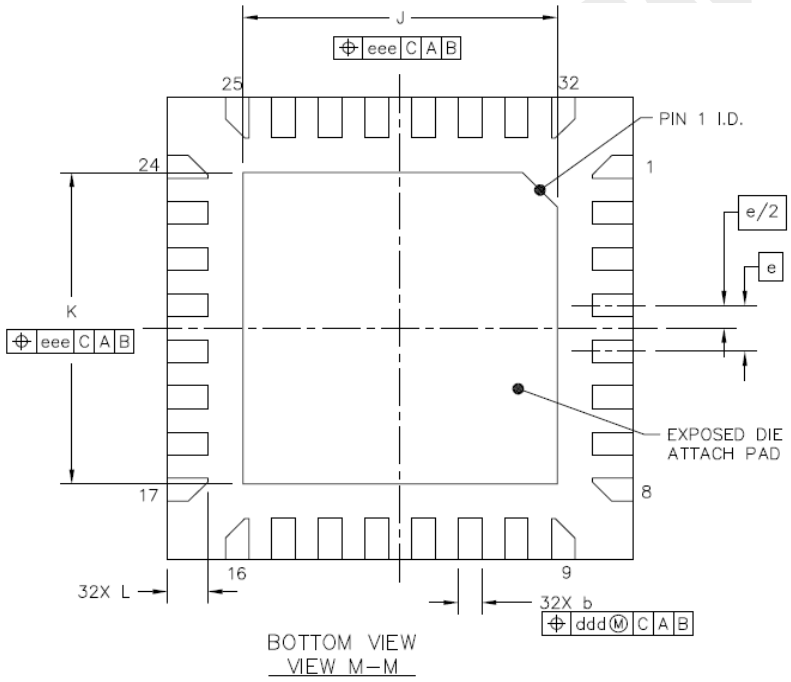
Table 17: Pinmux for SV6158

Name	Pin No.	Dir	PU/PD	SMAC(SDIO)
GPIO00	7	I	F	UART0_RXD
GPIO01	8	O	F	UART0_TXD
GPIO12	11	I/O	F	Strap
GPIO14	18	O	F	Wi-Fi_WAKEUP_Host
GPIO17	19	I/O	F	SD_DATA2
GPIO18	20	I/O	F	SD_DATA3
GPIO19	21	I/O	F	SD_CMD
GPIO20	22	I	F	SD_CLK
GPIO21	23	I/O	F	SD_DATA0
GPIO22	24	I/O	F	SD_DATA1
GPIO33	27	O	F	RX_IRQ(out_band)
GPIO36	30	N/A	F	UART2_RXD
GPIO37	31	N/A	F	UART2_TXD

9 PACKAGE INFORMATION

4 x 4 mm (body size), 0.4mm pitch QFN-32





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.6	2.7	2.8
	Y	K	2.6	2.7	2.8
LEAD LENGTH		L	0.3	0.35	0.4
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 11: QFN 4 x 4 mm Package Dimensions

10 ORDERING INFORMATION

The table below provides the ordering information of the SV6158.

Table 18: SV6158 Ordering Part Number

Part number	Package	Feature
SV6158	QFN32	Wi-Fi